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EXAMINER	
LEUNG, CHRISTINA Y	
ART UNIT	**PAPER NUMBER**
2633	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,693	KUNST ET AL.	
	Examiner	Art Unit	
	Christina Y. Leung	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10 and 13-20* is/are rejected.

7)☒ Claim(s) *4,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13, 14, and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Roberts (US 5,286,969 A).

Regarding claim 13, Roberts discloses a receiver (Figure 1) comprising:

means for receiving an optical signal and converting the optical signal to an electrical signal (photodiode 2; column 1, lines 66-68);

means for performing a linear-to-logarithmic conversion of the electrical signal to provide a first signal (including element 7 within power monitor 4; column 2, lines 30-39); and

means for converting the first signal from an analog to a digital format to provide an output signal (not explicitly shown in Figure 1, but Roberts discloses an analog-to-digital converter; column 2, lines 25-29).

Regarding claim 14, Roberts discloses that the output signal reports a relative strength of the optical signal in logarithmic units (column 1, line 68; column 2, lines 1-4).

Regarding claim 17, Roberts discloses a method of measuring optical power comprising:

receiving an optical signal (at photodiode 2);

converting the optical signal to an electrical signal (using photodiode 2); and

performing a linear-to-logarithmic conversion on the electrical signal to provide an output signal (using power monitor 4, particularly element 7; column 1, line 68; column 2, lines 1-13).

Regarding claim 18, Roberts disclose performing an analog-to-digital conversion on the output signal to provide a digital signal indicating the relative strength of the optical signal in logarithmic units (column 2, lines 1-4 and lines 21-29).

Regarding claim 19, Roberts discloses that the linear-to-logarithmic conversion comprises converting the electrical signal to a direct current voltage signal that is proportional to an optical power of the optical signal (column 2, lines 14-17) and converting the direct current voltage signal from linear values to logarithmic values to provide the output signal (column 2, lines 1-2, lines 11-13, and lines 21-39).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts in view of Oda (US 4,891,603 A).

Regarding claim 15, Roberts discloses a receiver as discussed above with regard to claim 13 including means for performing a linear-to-logarithmic conversion. Roberts further discloses transistors but does not specifically disclose that the logarithmic converter employs a logarithmic relationship between a base-emitter voltage and a collector current of a transistor.

However, Oda teaches a simple logarithmic conversion circuit (Figure 1) including a transistor 3. Oda further teaches that the circuit provides a logarithmic output based on the relationship between a base-emitter voltage and a collector current of a transistor (column 1, lines 11-58). It would have been obvious to a person of ordinary skill in the art to use the particular logarithmic converter circuitry taught by Oda as an engineering design choice of a simple and inexpensive way to provide the logarithmic output already disclosed by Roberts. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art. The system disclosed by Roberts already similarly utilizes a logarithmic relationship naturally arising from transistor connections.

Regarding claim 20, Roberts a method of measuring optical power as discussed above with regard to claim 17 including a step of performing a linear-to-logarithmic conversion and providing a logarithmic output. Roberts does not further specifically disclose that the output signal has a value defined by one of the equations recited in claim 20.

However, again Oda teaches a simple logarithmic conversion circuit (Figure 1) including a transistor 3. Oda further teaches that this logarithmic conversion circuit provides a logarithmic output based on a specific relationship between the base-emitter voltage (referred to as V by Oda) of the transistor and values of current (referred to as Ic and Is by Oda) flowing through terminals of the transistor (column 1, lines 24-34). Oda teaches that the relationship (and resulting logarithmic output) is defined by "$V = (kT/q) \times \ln(Ic/Is)$" (column 1, line 45), which is equivalent to the equation "$\Delta V_{BE} = (nKT/q) \times \ln (I1/I2)$" recited in claim 20.

Examiner notes that the voltage V taught by Oda is a base-emitter voltage although

claim 20 does not specifically recite that "V_{BE}" is necessarily a base-emitter voltage.

Again, it would have been obvious to a person of ordinary skill in the art to use the particular logarithmic converter circuitry taught by Oda as an engineering design choice of a simple and inexpensive way to provide the logarithmic output already disclosed by Roberts. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art. The system disclosed by Roberts already similarly utilizes a logarithmic relationship naturally arising from transistor connections.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts in view of Kawashima (US 3,700,918 A).

Regarding claim 16, Roberts discloses a receiver as discussed above with regard to claim 13 including means for performing a linear-to-logarithmic conversion. Roberts does not specifically disclose that the logarithmic converter employs a logarithmic relationship between a voltage and a current of a diode.

However, Kawashima teaches simple implementations of logarithmic conversion circuits (Figures 1a-c) including two with a transistor related to the one already disclosed by Roberts (Figures 1a and 1b) and another with a diode 4 (Figure 1c). Kawashima further teaches that the circuit in Figure 1c provides a logarithmic output based on the relationship between a voltage and a current of the diode (column 2, lines 42-66). It would have been obvious to a person of ordinary skill in the art to use the particular logarithmic converter circuitry with a diode as taught by Kawashima as an engineering design choice of a simple and inexpensive way to provide the logarithmic output already disclosed by Roberts. The claimed differences exist not as a result of

an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art. The system disclosed by Roberts already similarly utilizes a logarithmic relationship naturally arising from circuitry connections.

6. Claims 1, 2, 5-7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art in view of Roberts.

Regarding claim 1, Applicants' Admitted Prior Art (Figure 1, which is labeled "Prior Art" and described in Applicants' specification as "a conventional fiber optics receiver"; pages 1 and 2) discloses a receiver comprising:

a photodiode 106 that translates an optical signal into an electrical signal;

a first amplifier 108, coupled to the photodiode, that receives the electrical signal and provides a first signal;

an analog-to-digital converter 112 that converts the signal output from the amplifier to a digital output signal.

The optical receiver shown in Applicants' Admitted Prior Art differs from the receiver recited in claim 1 only in that it lacks a converter that performs a linear-to-logarithmic conversion.

However, Roberts teaches an optical receiver (Figure 1), related to the one disclosed as Admitted Prior Art, including a photodiode 2 and an analog-to-digital converter (not shown in the Figure, but see column 2, lines 25-26). Roberts also teaches that the system is directed to monitoring the power of the received signal (column 1, lines 9-11); the Admitted Prior Art

system is also similarly disclosed as being directed to power monitoring (see Applicants' specification from page 1, line 26 to page 2, line 2).

Roberts further teaches a converter that performs a linear-to-logarithmic conversion of the signal from the photodiode to provide an output signal (element 7; column 2, lines 33-48).

It would have been obvious to a person of ordinary skill in the art to include a linear-to-logarithmic converter as taught by Roberts in the receiver disclosed by Applicants' Admitted Prior Art in order to generate an output signal proportional to the logarithm of the power of the optical signal received at the photodiode and thereby provide smaller range of the power monitor output signal corresponding to a larger range of receiver optical signal power (Roberts, column 2, lines 40-48). One in the art would have been motivated to include the logarithmic converter taught by Roberts in order to allow the power monitor to accurately and fully monitor a large range of possible power levels (Roberts, column 1, lines 29-43).

Regarding claim 2, Applicants' Admitted Prior Art discloses that the first amplifier provides a current to voltage conversion with a voltage level that is proportional to the average optical power received by the photodiode (specification, page 1, line 23-28).

Regarding claim 5, Applicants' Admitted Prior Art discloses a second amplifier 110, coupled to the photodiode, which converts the electrical signal into a second signal that contains a data stream (specification, page 1, lines 25-26).

Regarding claim 6, Applicants' Admitted Prior Art discloses that the first and second amplifiers are operational amplifiers (specification, page 1, line 20).

Regarding claim 7, Applicants' Admitted Prior Art discloses an optical fiber 102 coupled to the photodiode and providing the optical signal.

Regarding claim 10, Applicants' Admitted Prior Art discloses that the first signal is a direct current voltage signal that is proportional to an average power of the electrical signal (specification, page 1, lines 26-28).

7. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art in view of Roberts as applied to claim 1 above, and further in view of Oda.

Regarding claim 3, Applicants' Admitted Prior Art in view of Roberts describes a system as discussed above with regard to claim 1 including a linear-to-logarithmic converter and a logarithmic output. However, this system does not include an output signal specifically having a value defined by one of the equations recited in claim 3.

However, again, Oda teaches a simple logarithmic conversion circuit (Figure 1) including a transistor 3. Oda further teaches that this logarithmic conversion circuit provides a logarithmic output based on a specific relationship between the base-emitter voltage (referred to as V by Oda) of the transistor and values of current (referred to as Ic and Is by Oda) flowing through terminals of the transistor (column 1, lines 24-34). Oda teaches that the relationship (and resulting logarithmic output) is defined by "V = (kT/q) x ln(Ic/Is)" (column 1, line 45), which is the same as "ΔV_{BE} = (nKT/q) x ln (I1/I2)" recited in claim 20.

Examiner notes that the voltage V taught by Oda is a base-emitter voltage although claim 20 does not specifically recite that "V_{BE}" is necessarily a base-emitter voltage.

Again, it would have been obvious to a person of ordinary skill in the art to use the particular logarithmic converter circuitry taught by Oda as an engineering design choice of a simple and inexpensive way to provide the logarithmic output already included in the system

described by Applicants' Admitted Prior Art in view of Roberts. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art. The system described by Applicants' Admitted Prior Art in view of Roberts already similarly utilizes a logarithmic relationship naturally arising from transistor connections.

Regarding claim 8, Applicants' Admitted Prior Art in view of Roberts describes a system as discussed above with regard to claim 1 including a linear-to-logarithmic converter with transistors. However, this system does not include a logarithmic converter that employs a logarithmic relationship between a base-emitter voltage and a collector current of a transistor.

However, Oda teaches a simple logarithmic conversion circuit (Figure 1) including a transistor 3. Oda further teaches that the circuit provides a logarithmic output based on the relationship between a base-emitter voltage and a collector current of a transistor (column 1, lines 11-58). It would have been obvious to a person of ordinary skill in the art to use the particular logarithmic converter circuitry taught by Oda as an engineering design choice of a simple and inexpensive way to provide the logarithmic output already included in the system described by Applicants' Admitted Prior Art in view of Roberts. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art. The system described by Applicants' Admitted Prior Art in view of Roberts already similarly utilizes a logarithmic relationship naturally arising from transistor connections.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art in view of Roberts as applied to claim 1 above, and further in view of Kawashima.

Regarding claim 9, Applicants' Admitted Prior Art in view of Roberts describes a system as discussed above with regard to claim 1 including means for performing a linear-to-logarithmic conversion. However, this system does not include a logarithmic converter that specifically employs a logarithmic relationship between a voltage and a current of a diode.

However, Kawashima teaches simple implementations of logarithmic conversion circuits (Figures 1a-c) including two with a transistor related to the one already taught by Roberts (Figures 1a and 1b) and another with a diode 4 (Figure 1c). Kawashima further teaches that the circuit in Figure 1c provides a logarithmic output based on the relationship between a voltage and a current of the diode (column 2, lines 42-66). It would have been obvious to a person of ordinary skill in the art to use the particular logarithmic converter circuitry with a diode as taught by Kawashima as an engineering design choice of a simple and inexpensive way to provide the logarithmic output already included in the system described by Applicants' Admitted Prior Art in view of Roberts. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art. The system described by Applicants' Admitted Prior Art in view of Roberts already similarly utilizes a logarithmic relationship naturally arising from circuitry connections.

Allowable Subject Matter

9. Claims 4, 11, and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

The prior art, including Applicants' Admitted Prior Art, Roberts, Oda, and Kawashima, does not specifically disclose or fairly teach a system with all the elements and limitations in the combination recited by claims 4, 11, and 12 (and including all the limitations of their respective parent claim(s)), particularly wherein the final output of the analog-to-digital convert is based on a difference in the measure of an output when a current I1 or voltage V_{DC} is applied in the logarithmic converter first and an output when a current I2 or voltage V_{REF} is subsequently applied in the logarithmic converter (as recited in claim 4), or particularly wherein the logarithmic converter includes the specifically connected elements as recited in claims 11 and 12 (including a second amplifier that alternatively provides a first signal or a reference signal as an output, a first transistor, a resistor, a second transistor, and a current mirror or third transistor).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christina Y Leung
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